L60 ANSWER 4 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:900947 HCAPLUS
TI Non-volatile semiconductor memory cell and method for its production
IN Ludwig, Christoph; Schrems, Martin
PA Infineon Technologies Ag, Germany
PI US 2002098648 A1 20020725 US 2002-13264 20020404 <--
PRAI DE 1999-19926500 A 19990610 <--
WO 2000-DE1898 W 20000609
AB The invention relates to a nonvolatile semiconductor memory cell and to a method for its production according to which a floating gate is produced by standard methods in a self-adjusting manner. The use of TiO2 or WOx as the **dielec. layer** between a control gate and the floating gate results in a sufficiently great capacitive coupling factor and gives a semiconductor memory cell of very small dimensions.
IT 78-10-4, TEOS 1314-35-8, Tungsten oxide, processes 7440-21-3, Silicon, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes 12058-38-7, Tungsten nitride (WN) **13463-67-7**, Titanium dioxide, processes 25583-20-4, Titanium nitride (TiN)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(non-volatile semiconductor memory cell and method for production)
IT **13463-67-7**, Titanium dioxide, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(non-volatile semiconductor memory cell and method for production)
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

L60 ANSWER 5 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:881466 HCAPLUS
TI Non-volatile semiconductor memory cell, comprising a metal-oxide dielectric, and a method for producing the same.
IN Ludwig, Christoph; Schrems, Martin
PA Infineon Technologies A.-G., Germany
PI US 6580118 B2 20030617 US 2001-13271 20011210 <--
PRAI DE 1999-19926108 A 19990608 <--
WO 2000-DE1866 W 20000606
AB The invention relates to a nonvolatile semiconductor memory cell and a method for producing the same. In the method, a conventional, **dielec.** ONO **layer** is replaced by an extremely thin metal-oxide layer, consisting of WOx and/or TiO2. An addnl. improvement in the integration d. and the control voltage necessary for the semiconductor memory cell is achieved as a result of the high relative dielec. constant of these materials.
IT 78-10-4, TEOS 409-21-2, Silicon carbide, processes 1303-00-0, Gallium arsenide, processes 7440-21-3, Silicon, processes 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes 11148-21-3 12033-89-5, Silicon nitride (Si3N4), processes 12627-41-7, Tungsten silicide **13463-67-7**, Titania, processes 25583-20-4, Titanium nitride 37359-53-8, Tungsten nitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(non-volatile semiconductor memory cell, comprising a metal-oxide dielec., and a method for producing the same.)
IT **13463-67-7**, Titania, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(non-volatile semiconductor memory cell, comprising a metal-oxide dielec., and a method for producing the same.)
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

L60 ANSWER 7 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:508173 HCAPLUS
TI Method of fabricating transistor having a metal gate and a gate **dielectric layer** with a high **dielectric** constant
IN Lou, Chine-gie
PA Worldwide Semiconductor Manufacturing Corp., Taiwan
PI US 6093590 A 20000725 US 1999-395109 19990914 <--
PRAI US 1999-395109 19990914 <--
AB A method of fabricating a transistor is claimed. A 1st **dielec. layer** with a high **dielec.** constant is formed on a substrate. An oxide **layer** is formed on the 1st **dielec . layer.** A Si nitride layer is formed on the oxide layer. The Si nitride **layer,** the oxide **layer,** and the 1st **dielec. layer** are patterned to form a dummy gate structure. A spacer is formed on a sidewall of the dummy gate structure. The spacer and the dummy gate structure together form a dummy gate. An ion implantation step with the dummy gate serving as a mask and a thermal annealing step were performed to form a source region and a drain region on opposite sides of the dummy gate in the substrate. A 2nd **dielec. layer** is formed next to the spacer. A top surface of the 2nd **dielec. layer** is approx. level with a top surface of the dummy gate structure. The Si nitride layer is removed. A nitridation process was performed to convert the oxide layer into a nitride layer. A metal barrier layer is formed over the substrate to cover the 2nd **dielec. layer,** the spacer, and the nitride **layer.** A metal layer is formed on the metal barrier layer. A planarization process was performed to remove a portion of the metal layer and the metal barrier layer to form a metal gate. A top surface of the metal gate is level with a top surface of the 2nd **dielec. layer.**
ST MOSFET MISFET fabrication high **dielec** const **film**
IT 25583-20-4, Titanium mononitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(barrier; method of fabricating transistor having metal gate and gate **dielec. layer** with high **dielec.** constant)
IT **1314-61-0,** Tantalum pentoxide 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of fabricating transistor having metal gate and gate **dielec. layer** with high **dielec.** constant)
IT **1314-61-0,** Tantalum pentoxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of fabricating transistor having metal gate and gate **dielec. layer** with high **dielec.** constant)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

L60 ANSWER 10 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:76946 HCAPLUS
TI Fabricating a high-dielectric-constant interpolysilicon dielectric structure for a low-voltage nonvolatile memory
IN He, Yue-song; Ibok, Effiong
PA Advanced Micro Devices, Inc., USA
PI US 6020238 A 20000201 US 1997-978107 19971125 <--
PRAI US 1997-978107 19971125 <--
AB A method of fabricating an interpolysilicon dielec. structure in a nonvolatile memory includes forming a nitride layer on a floating gate and a high-**dielec.**-constant **layer** on the nitride **layer**. A control gate may be formed directly on the high- **dielec.**-constant **layer**, or on a thin **layer** of an oxide or an oxynitride on the high-**dielec.**-constant **layer** .
IT **1314-61-0**, Tantalum oxide (Ta2O5) 7631-86-9, Silica, processes 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, processes **13463-67-7**, Titanium dioxide, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a high-dielec.-constant interpolysilicon dielec. structure for a low-voltage nonvolatile memory containing)
IT **1314-61-0**, Tantalum oxide (Ta2O5) **13463-67-7**, Titanium dioxide, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a high-dielec.-constant interpolysilicon dielec. structure for a low-voltage nonvolatile memory containing)
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

L60 ANSWER 12 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:405201 HCAPLUS
TI Fabrication of high dielectric constant insulator for gate contact for semiconductor devices
IN Gardner, Mark I.; Fulford, H. Jim
PA Advanced Micro Devices, Inc., USA
PI US 6258675 B1 20010710 US 1997-993766 19971218
PRAI US 1997-993766 A 19971218 <--
AB A gate insulator having a high dielec. constant is disclosed. In one embodiment of the invention, the method includes three steps. In the 1st step, a gate insulator layer is formed on a substrate. The gate insulator layer includes at least one **layer**, having a high **dielec** . constant In the 2nd step, a gate conductor is formed on the gate insulator layer, the gate conductor masking a portion of the gate insulator layer. In the 3rd step, the gate insulator layer is removed, except for the portion masked by the gate conductor. In a particular embodiment, the gate insulator is formed by depositing Si3N4, then Ta2O5 or TiO2, then Si3N4. Then depositing and patterning gate polysilicon. Then oxidizing polysilicon. Then etching the two uppermost gate insulator layers. Then implanting and annealing source and drain. Then remove the oxide which was formed on the polysilicon. Results in upper gate insulator layers being wider than gate polysilicon.
IT **1314-61-0**, Tantalum oxide (Ta2O5) 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride (Si3N4), processes **13463-67-7**, Titanium oxide (TiO2), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of high dielec. constant insulator for gate contact for semiconductor devices)
IT **1314-61-0**, Tantalum oxide (Ta2O5) **13463-67-7**, Titanium oxide (TiO2), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of high dielec. constant insulator for gate contact for semiconductor devices)

L60 ANSWER 14 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:761578 HCAPLUS
TI Modified gate structure for nonvolatile memory and its method of fabricating the same
IN Chou, Kuo-Yu
PA Winbond Electronics Corp., Taiwan
PI US 5994734 A 19991130 US 1998-120490 19980721 <--
PRAI US 1998-120490 19980721 <--
AB A modified gate structure for a nonvolatile memory device is formed over a substrate. The modified gate structure from bottom to top comprises a 1st **dielec. layer**, a 1st conductive **layer**, a 2nd **dielec. layer** formed on said 1st conductive **layer**, a 3rd **dielec. layer**, a refractory metal **layer**, and a 2nd conductive layer. The 3rd **dielec. layer** is made of Ta oxide or BST, and the refractory metal layer can be made of W, Pt, Ti, Mo, and Ta.
IT **1314-61-0**, Tantalum pentoxide 7439-98-7, Molybdenum, processes 7440-06-4, Platinum, processes 7440-25-7, Tantalum, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes 37303-24-5, Barium strontium titanium oxide (Ba0-1Sr0-1TiO3)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in modified gate structure for nonvolatile memory and method of fabricating same)

L60 ANSWER 15 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:439371 HCAPLUS
TI Electronic components with doped metal oxide dielectric materials and a process for making MOS devices with doped metal oxide dielectric materials
IN Lee, Woo-hyeong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
PI US 5923056 A 19990713 US 1998-41434 19980312 <--
JP 11297867 A2 19991029 JP 1999-65742 19990312 <--
PRAI US 1996-27612P P 19961010 <--
AB A doped, metal oxide dielec. material and electronic components made with this material are disclosed. The metal oxide is a Group III or Group VB metal oxide (e.g. Al2O3, Y2O3, Ta2O5 or V2O5 and the metal dopant is a Group IV material (Zr, Si, Ti, and Hf)). The metal oxide contains .apprx.0.1 to .apprx.30 weight% of the dopant. The doped, metal oxide dielec. of the present invention was used in a number of different electronic components and devices. For example, the doped, metal oxide dielec. was used as the gate dielec. for MOS devices. The doped, metal oxide dielec. is also used as the inter-poly dielec. material for flash memory devices.
IT **Dielectric films**
MOS devices
MOSFET (transistors)
(electronic components with doped metal oxide **dielec.** materials and process for making MOS devices with doped metal oxide dielec. materials)
IT **1314-36-9**, Yttrium oxide (Y2O3), uses **1314-61-0**, Tantalum oxide (Ta2O5) 1314-62-1, Vanadium oxide (V2O5), uses **1344-28-1**, Aluminum oxide (Al2O3), uses
RL: DEV (Device component use); USES (Uses)
(electronic components with doped metal oxide dielec. materials and process for making MOS devices with doped metal oxide dielec. materials)

L60 ANSWER 16 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:490453 HCAPLUS
TI Stacked floating gate memory device
IN Clemens, James Theodore; Lee, Woo Hyong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
PI JP 10189921 A2 19980721 JP 1997-277485 19971009 <--
PRAI US 1996-27612P P 19961010 <--
US 1996-871024 A 19961010 <--
AB The invention relates to a stacked floating gate memory device, i.e., flash memory, e.g., EPROM, wherein the IPD (inter-poly **dielec.**) **layer** interposed between the floating and control gates enables a erasing voltage ≥ 5 V.
IT **1314-36-9**, Yttria, uses **1314-61-0**, Tantalum pentoxide
1344-28-1, Alumina, uses
RL: DEV (Device component use); USES (Uses)
(IPD for stacked floating gate memory device)

AN 1996:483233 HCAPLUS
TI Nonvolatile semiconductor memory devices containing floating-gate transistor cell
IN Oota, Tomoyuki
PA Nippon Electric Co, Japan
PI JP 08153811 A2 19960611 JP 1994-294865 19941129
US 5739566 A 19980414 US 1995-564445 19951129 <--
PRAI JP 1994-294865 19941129 <--
AB The devices have memory cells of a floating-gate transistor, which consists of a 1st gate insulator, a 1st floating gate electrode (e.g., doped polycryst. Si-TiN laminate), an interlayer insulator, a 2nd floating gate electrode (e.g., concave-shaped) connecting to the 1st floating gate electrode through the contact holes of the interlayer insulator, a 2nd gate insulator (e.g., Ta2O5, SrTiO3, (Ba,Sr)TiO3, or PZT), and a control electrode, successively formed on a substrate. The devices may have a 1st wiring (bit wire) between the 1st and 2nd floating gate electrodes, which is insulated from the floating gate electrodes and a gate electrode as a 2nd wiring (word wire). The devices may have a 3rd wiring with resistance lower than the 1st wiring on the 2nd wiring via an interlayer insulator, which connects to the 1st wiring. The devices have low operation voltage.
IT **1314-61-0**, Tantalum oxide 12060-59-2, Strontium titanate 12626-81-2, PZT 37305-87-6, Barium strontium titanate
RL: DEV (Device component use); USES (Uses)
(gate insulator; flash EEPROM for low operation voltage)

L60 ANSWER 19 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:386036 HCAPLUS
TI Semiconductor memory devices and manufacture thereof
PA Goldstar Co., Ltd., S. Korea

PI	JP 06196654	A2	19940715	JP 1993-213379	19930804 <--
	KR 9604462	B1	19960406	KR 1992-14195	19920807
	US 5552337	A	19960903	US 1994-301437	19940909 <--
PRAI	KR 1992-14195	A	19920807 <--		
	US 1993-103059	B3	19930809		

AB The device has a capacitor which has a 1st electrode (e.g., a layer doped with Si) on a semiconductor substrate, a Ta2O5 **dielec. film** doped with Si (e.g., as Si and/or Si oxide) thereon, and a 2nd electrode on the **dielec. layer**. The **dielec. layer** may be formed from Ta(EtO)5 and O2 at ≤400°, and doping may be made by supply of the Ta source simultaneously with a Si source and/or diffusion of Si from the underlying layer. The **dielec. film** decreases leakage current.

IT **1314-61-0P**, Tantalum oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(**film**, doped with silicon; for **dielec. films** in capacitors of memory devices)

L60 ANSWER 21 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1993:529716 HCAPLUS
TI Self-aligned stacked gate EPROM cell using tantalum oxide control gate dielectric
IN Yoon, Euisik; Bergemont, Albert M.; Kovacs, Ronald F.
PA National Semiconductor Corp., USA
PI EP 528564 A3 19950308
PRAI US 1991-747663 A 19910820 <--
AB A process flow fabricates a self-aligned stacked gate EPROM cell that uses a CVD Ta oxide film to replace ONO as a control gate dielec. As the control gate, W replaces polysilicon. Both the dielec. deposition and cell definition steps of the process flow are performed in a back-end module to improve dielec. integrity in the memory cells by minimizing high-temperature exposure of the Ta oxide film.
IT **1314-61-0**, Tantalum oxide (Ta2O5)
RL: TEM (Technical or engineered material use); USES (Uses)
(control gate **dielec.**, in self-aligned **stacked** gate memory cell)

L60 ANSWER 23 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1985:141881 HCAPLUS Full-text
TI Thin-film integrated device
IN Nomura, Koji; Ogawa, Hisahito; Abe, Atsushi; Nitta, Tsuneharu
PA Matsushita Electric Industrial Co., Ltd. , Japan

PI	WO 8403992	A1	19841011	WO 1984-JP145	19840329 <--
	JP 05063947	B4	19930913	JP 1983-57552	19830331
	JP 04006277	B4	19920205	JP 1983-98343	19830602
	EP 139764	A1	19850508	EP 1984-901397	19840329 <--
PRAI	JP 1983-57552		19830331 <--		
	JP 1983-98343		19830602 <--		

AB In a thin-film integrated device having ≥1 thin-film element(s) on an insulator substrate, the thin-film element(s) consists of an insulator thin film of a sputter-deposited complex oxide containing Ta and Al. The insulator **film** has a high **dielec.** constant, high **dielec.**-breakdown field strength, and low leakage current. Optionally, the integrated device may be comprised of a ZnS electroluminescent display device and thin-film element(s) may consist of a thin-film capacitor, CdSe FET, and/or LED.

IT **1314-61-0D**, solid solns. with alumina **1344-28-1D**, solid solns. with tantalum oxide
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(elec. insulators, for thin-film integrated devices)

L70 ANSWER 6 OF 15 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-259779 [23] WPIX Full-text
TI Thin **film** capacitor for ferroelectric **memory** has thin **dielectric film** with **lattice constant** , curie temperature and unit crystal lattices, satisfying specific relation.
PA (TOKE) TOSHIBA KK
PI JP 11340429 A 19991210 (200023)* 9p H01L027-10
PRAI JP 1998-144031 19980526
AB JP 11340429 A UPAB: 20000516
NOVELTY - A thin **dielectric film** (3) is **sandwiched** between a pair of electrodes (2,4). The **lattice constant** and curie temperature of the entire dielectric and along its thickness are denoted as cb, Tc K, cf, Tf K respectively where cf-cb divided by cb at least 0.02, Tf-Tc at least 250 deg. C. DETAILED DESCRIPTION - The number of unit crystal lattices `N' of the **dielectric film** along its thickness is lesser than or equals 34. An epitaxial growth of perovskite-type crystal structured thin **dielectric film** is performed on the surface [100] or [001] of a cubic or tetragonal system electrode (2). The **dielectric film** is made-up of AB03, where A is Ba, Sr, or Ca, B is Ti, Zr, Hf, Sn, Mg1/3 Nb2/3, Mg1/3 Ta2/3, Ni1/3 Ta2/3 or Co1/3 Nb2/3 or Co1/3 Ta2/3 where 1/3 and 2/3 are Sc, Ta or Nb. Another electrode is formed on the **dielectric film**. An INDEPENDENT CLAIM is also included for ferroelectric **memory** manufacturing method.
USE - For ferroelectric **memory** e.g. **DRAM**.
ADVANTAGE - Curie temperature is raised by introducing distortion to crystal lattice of **dielectric film**, thus ferroelectric characteristic is maintained. By utilization of thin **dielectric film**, heat release per unit area of **memory** cell is suppressed during repeating polarization inversion. Fatigue resistance of **memory** is improved. By thin **dielectric film**, anti-voltage is reduced, driving voltage of capacitor is low, operating voltage of **memory** is reduced. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of capacitor. (2,4) Electrodes; (3) Thin **dielectric film**.

L70 ANSWER 7 OF 15 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1999-484962 [41] WPIX Full-text
TI Dielectric element used in LSI, **DRAM** - includes **dielectric film** of perovskite structure compound laid on electrode layer having different **lattice constant**, to perform **lattice** matching.
PA (TAIO) TAIYO YUDEN KK
PI JP 11204745 A 19990730 (199941)* 6p H01L027-10
PRAI JP 1998-13251 19980108
AB JP 11204745 A UPAB: 19991011
NOVELTY - A **dielectric film** of perovskite structure compound is coated on an electrode layer that has a different **lattice constant**, to perform **lattice** matching.
USE - In LSI, **DRAM**, microwave monolithic IC, ferroelectric **RAM**.
ADVANTAGE - By coating a **dielectric film** of high **dielectric constant**, a homogeneous and stable dielectric element is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of dielectric element.
Dwg.1/3

L70 ANSWER 8 OF 15 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1999-220891 [19] WPIX Full-text
TI **Dielectric** thin **film** for capacitor - has mean crystal grain diameter of oxide dielectric set at predetermined value.
PA (SONY) SONY CORP
PI JP 11054710 A 19990226 (199919)* 10p H01L027-04
PRAI JP 1997-213717 19970807
AB JP 11054710 A UPAB: 19990518
NOVELTY - The mean crystal grain diameter of an oxide dielectric of a polycrystal in a **dielectric** thin **film** is given as 40 nm or less. The **dielectric** thin **film** is made from the oxide of two or more elements of groups IIa, IVa, Va or IVb or Vb.

DETAILED DESCRIPTION - Magnesium, calcium, strontium and barium are selected from IIa group elements. Titanium and zirconium are selected from IVa group elements, lead and tin from IVb group elements and bismuth from Vb group elements.

USE - For capacitor used in **DRAM**.

ADVANTAGE - Controls crystal grain diameter due to oxide dielectric elements selection with diameter set to 40 nm or less, effecting high **dielectric constant**.

DESCRIPTION OF DRAWING(S) - The figure shows characteristic view of mean crystal grain diameter and **lattice constant** ratio.
Dwg.3/15

L70 ANSWER 10 OF 15 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1998-278173 [25] WPIX Full-text
TI Thin **film** capacitor for semiconductor **memories** - forms **dielectric film** epitaxially, over base electrode of cubic/tetragonal structure, formed film crystal **lattice constants** having defined ratios with base electrode structure.
IN ABE, K; FUKUSHIMA, N; IZUHA, M; KAWAKUBO, T; KOMATSU, S; SANO, K
PA (TOKE) TOSHIBA KK
PI JP 10093050 A 19980410 (199825)* 25p H01L027-108
KR 97063723 A 19970912 (199840) H01L027-10
US 5889299 A 19990330 (199920) H01L029-76 <--
KR 228038 B1 19991101 (200110) H01L027-10
PRAI JP 1996-196198 19960725; JP 1996-34868 19960222
AB JP 10093050 A UPAB: 19980624
The construction of thin **film** capacitor involves deposition of the **dielectric film** (3) epitaxially, over the base electrode (2) in turn supported by the substrate (1). Upper electrode (4) formed over the **dielectric film** completes the capacitor formation. The base electrode is of cubic or tetragonal (001) structure and where a perovskite cubic system is employed, the unit lattice volume (Vo) is ao3, where ao is the **lattice constant**.

The **dielectric film** epitaxially formed, has a unit lattice volume (V) covered by the **lattice constants** a=b is not equal to c and is given as a2c. These volume are governed by the relation V/Vo>=1.01. The film **lattice constant** conform to the relation c/a>=1.01 where c is the direction perpendicular to the film surface and ao/a <=1.002.

ADVANTAGE - In semiconductor **DRAM** type **memories**. Controls frequency dependence of **dielectric constant** and remnants. Produces high **dielectric constant films** as well as ferroelectric thin films reliably. Dwg.1/28

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     FILE 'REGISTRY' ENTERED AT 09:02:56 ON 18 FEB 2004
L1            8 S AL2O3/MF
L2          127 S AL.O/MF
L3            3 S O3Y2/MF
L4           65 S O.Y/MF
L5           27 S O.SI.ZR/MF
L6            0 S O.SI.HF/MF
L7            0 S O.HF.SI/MF
L8            8 S HF.O.SI/MF
L9            0 S O3LA2/MF
L10           4 S LA2O3/MF
L11          21 S LA.O/MF
L12          14 S O2ZR/MF
L13         109 S O.ZR/MF
L14           7 S HFO2/MF
L15          25 S HF.O/MF
L16           3 S O5TA2/MF
L17         106 S O.TA/MF

     FILE 'DPCI' ENTERED AT 09:03:00 ON 18 FEB 2004
L18           1 S US 6008091/PN
L19             SEL L18 1- PN :        5 TERMS
L20           1 S L19
L21             SEL L18 1- PN.G :        8 TERMS
L22             SEL L18 1- PN.D :        9 TERMS
L23           8 S L21/PN
L24           9 S L22/PN
L25          17 S (L23 OR L24)
L26             SEL L25 1- PN.G :      600 TERMS
L27         474 S L26/PN
L28             SEL L27 1- PRN :      715 TERMS

     FILE 'REGISTRY' ENTERED AT 09:09:24 ON 18 FEB 2004
L29           1 S O3PR2/MF
L30          53 S O.PR/MF
L31          17 S O2TI/MF
L32         280 S O.TI/MF
L33           0 S SIO2/MF
L34          48 S O2SI/MF
L35           0 S O2.SI/MF
L36         346 S O.SI/MF
L37        3227 S AL O/ELF
L38        1737 S O Y/ELF
L39         102 S O SI ZR/ELF
L40           0 S O SI HF/ELF
L41          28 S HF O SI/ELF
L42         282 S LA O/ELF
L43        1058 S O ZR/ELF
L44         163 S HF O/ELF
L45         315 S O TA/ELF
L46          88 S O PR/ELF
L47         991 S O TI/ELF
L48       19869 S O SI/ELF
L49        7706 S ((L29 OR L30 OR L31 OR L32)) OR ((L37 OR
                L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR L44 OR L45 OR L46 OR
                L47)) OR ((L1 OR L2 OR L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9
                OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17))
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     FILE 'HCAPLUS, WPIX' ENTERED AT 09:12:32 ON 18 FEB 2004
L50         847 S L28
L51      157313 S (DIELEC? OR KAPPA OR K OR PERMIT######)(6A)
                (STACK? OR SANDWICH? OR LAYER? OR MULTILAYER? OR FILM? OR
                LAMINA######)
L52      165814 S (FORBIDDEN OR ENERG####)(2A)(GAP# OR
                BAND#) OR BANDGAP# OR EG OR LATTICE#(2A) CONSTANT#

     FILE 'REGISTRY' ENTERED AT 09:15:28 ON 18 FEB 2004
L53             SEL L49 1- RN :    7706 TERMS

     FILE 'HCAPLUS, WPIX' ENTERED AT 09:20:31 ON 18 FEB 2004
L54      428451 S L53
L55         847 S L28
L56          23 S L54 AND L55
L57           0 S L56 AND L52
L58          19 S L56 AND L51
L59          23 S (L56 OR L57 OR L58)
L60          23 DUP REMOVE L59 (0 DUPLICATES REMOVED)
L61        1924 S L51 AND L52
L62      695072 S (H01L021? OR H01L029?)/IC OR (L03-G04A OR
                L04-C12A OR U11-C18B5 OR U12-D02A1 OR U12-Q OR U13-D02 OR
                U141-A03B7)/MC
L63     1354770 S (L03 OR L04 OR U11 OR U12 OR U13 OR
                U14)/DC
L64          351 S L61 AND (L62 OR L63)
L65      153624 S DIELECT?(2A) CONSTANT? OR (HIGH OR
                LOW)(2A)(K OR PERMITT####### OR KAPPA)
L66           67 S L64 AND L65
L67      741186 S MEMOR### OR PROM OR PROMS OR ROMS OR ROM
                OR RAM OR SRAM OR DRAM OR EPROM OR EPROMS OR EEPROM OR EEPROMS
                OR STOR###(2A)(INFORMATION OR DATA) OR (NONVOLATILE OR
                FLASH)(2A) MEMOR###
L68          17 S L66 AND L67
L69          17 S L68 NOT L60
L70          15 DUP REMOVE L69 (2 DUPLICATES REMOVED)
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